

Modelling Router Behaviour Using External Measurements

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Extended Abstract

Knowledge of the internal workings of a router is important to get the full understanding of what goes on in a network, and to interpret the results from measurements. Especially it is important to understand when and why delay occurs, and what constitutes the delay. So far, external measurements on the input and output link have been used to measure the single-hop delay through a router. This requires heavy instrumentation as well as strict synchronization between measurement devices on the input and output ports. Contrary, investigating single-hop delay using measurement equipment on the output ports only may be of great use, eliminating the need for synchronization.

A generic model of a router is developed, where the functionality and resources of a router are split into four different parts; Router processing power which is used for router forwarding table lookup and decisions regarding the correct output port. Internal buffering space, both for input and output buffering. Internal bus capacity used for packet transmission from input buffers to the correct output buffer. And finally, the capacity on the outgoing links. It is then clear that the delay or sojourn time in the router experienced by a packet is partly packet size dependent due to transmission time and partly packet size independent due to router table lookup and buffering (assuming that the buffer allocation scheme is packet size independent). Input buffering, internal bus transmission time and the processing time is regarded as one measure, thus becoming dependent on the packet size. This measure is called router transit time. Internal bus transmission, processing time and the transmission time on the outgoing link are independent of the load on the router. Input and output buffering time however, is greatly influenced by the router load, with cross traffic causing buffer delay.

Occasional packets may also experience severe delays caused by routers taking a break in the forwarding process to update the routing tables or for garbage collection. This can be seen because the maximum delay experienced by packets can be high even in periods of low loads and idle output links. A third possibility for this delay may be head-of-line blocking experienced in some routers.

Some analytical models of the router may also be given for different regimes. In the limiting case for these regimes some of the resources in the router may be viewed as unlimited. Three different regimes are therefore identified for analysing the router analytically; Output link capacity limited, memory size limited or processing time limited.

First, by introducing a very big buffer and a fast enough processor such that no input queuing is experienced, the output links are the only restriction. The router may then be modelled by a M/G/1 queuing system, where the delay experienced by a packet is output queuing delay, transmission time and router transit time. Pollaczek-Khintchine formula may then be used to calculate the average

queuing delay. Because of the simple relationship between the average length of the busy period, the load and the average packet length, investigations of the busy periods on the output link are used to find the second-order moment of the packet size distribution needed in Pollaczek-Khintchine. Also, when the processing power is unrestricted, measurements can be used to find a linear relationship between packet size and router transit time. When this is found, the delay for a packet may be found using measurements on the outgoing link only.

Second, letting the buffer size be the limited resource, the packet loss is of great interest. This issue is complicated by the fact that packets are of different sizes. The noticeable difference on the packet size distribution on e.g. an uplink and a downlink means that the packet loss rates found from the classical formulas using number of packets in a full buffer are unrealistic. The buffer space in current routers are divided into chunks of varying sizes and hence measurements and analytical computations may be used to get an understanding of how many packets are needed to fill a buffer, depending on the packet size distribution. The buffer chunk sizes in Cisco routers are used for this analysis.

At last, the capacity on the outgoing links and the buffer capacity may be large, causing the processing power to restrict the throughput of the router. In this case, the delay experienced by a packet is due only to router transit time and output link transmission time. A different relationship between the packet size and the router transit time are then given, where also the input buffering contributes to the single-hop delay.

These regimes are each investigated in an operational setup using the Q2S Testbed. DAG-cards are used for traffic generation and passive measurements.